In the Claims

Amendments to the Claims:

1. (amended) A method of forming an aligned dual damascene opening, comprising the sequential steps of:

providing a structure having a metal structure formed thereover;

forming a layer stack over the metal structure; the layer stack comprising, in ascending order: a bottom etch stop layer; a lower dielectric material layer; a middle etch stop layer; a middle dielectric material layer; and an upper dielectric layer; wherein:

the lower and middle dielectric layers are comprised of the same material; or

the bottom etch stop layer, the middle etch stop layer and the upper dielectric layer are comprised of the same material;

patterning the upper dielectric layer to form an opening exposing a portion of the underlying middle dielectric material layer; the opening having a width;

forming a patterned mask layer over the patterned upper dielectric layer leaving exposed opposing portions of the patterned upper dielectric layer;

patterning the middle dielectric material layer to form an opening therein using the patterned mask layer and the exposed portions of the upper dielectric

layer as masks; the middle dielectric material layer opening exposing a portion of the middle etch stop layer;

removing the middle etch stop layer at its exposed portion to form a patterned middle etch stop layer having an opening exposing a portion of the lower dielectric material layer;

simultaneously patterning:

the patterned middle dielectric material layer using the patterned upper dielectric layer as a mask to form an inchoate upper trench opening; and

the lower dielectric material layer using the patterned mask layer and the patterned middle etch stop layer as masks to form an inchoate lower via opening aligned with the inchoate upper trench opening; the inchoate lower via opening exposing a portion of the underlying bottom etch stop layer;

removing the patterned mask layer; and

removing the patterned upper dielectric material layer, the exposed portions of the patterned middle etch stop layer and the exposed portion of the bottom etch stop layer to convert:

the inchoate upper trench opening into a final upper trench opening; and

the inchoate lower via opening into a final lower via opening;

to form the aligned dual damascene opening.

2. (original) The method of claim 1, wherein the structure is a semiconductor wafer.

3. (original) The method of claim 1, wherein the structure is comprised of silicon or germanium.

4. (original) The method of claim 1, wherein the metal structure is comprised of copper, aluminum, gold, an aluminum copper alloy or an aluminum silica copper alloy; the bottom etch stop layer is comprised of a dielectric material such as SiN, SiC, SiCO, SiCN, a combination of SiC(O) and SiC(N) or BLOK; the lower dielectric material layer is comprised of a dielectric material such as FTEOS or low-k dielectric materials; the middle etch stop layer is comprised of a dielectric material such as SiN, SiC(O), SiC(N), , a combination of SiC(O) and SiC(N) or BLOK; the middle dielectric material layer is comprised of a dielectric material such as FTEOS or low-k dielectric materials; and the upper dielectric layer is comprised of a dielectric layer such as SiN, SiC(O), SiC(N), , a combination of SiC(O) and SiC(N) or BLOK.

5. (original) The method of claim 1, wherein the metal structure is comprised of copper; the bottom etch stop layer is comprised of a combination of SiC(O) and SiC(N); the lower dielectric material layer is comprised of FTEOS or a low-k

dielectric material; the middle etch stop layer is comprised of SiN; the middle dielectric material layer is comprised of FTEOS or a low-k dielectric material; and the upper dielectric layer is comprised of SiN.

6. (original) The method of claim 1, wherein the lower and middle dielectric layers are comprised of the same material.

7. (original) The method of claim 1, wherein the bottom etch stop layer, the middle etch stop layer and the upper dielectric layer are comprised of the same material.

8. (original) The method of claim 1, wherein the metal structure has a thickness of from about 1000 to 5000Å; the bottom etch stop layer has a thickness of from about 250 to 1000Å; the lower dielectric material layer has a thickness of from about 2000 to 6000Å; the middle etch stop layer has a thickness of from about 250 to 1000Å; the middle dielectric material layer has a thickness of from about 2000 to 6000Å; and the upper dielectric layer has a thickness of from about 250 to 1000Å.

9. (original) The method of claim 1, wherein the metal structure has a thickness of from about 2000 to 3000Å; the bottom etch stop layer has a thickness of from about 400 to 600Å; the lower dielectric material layer has a thickness of from about 3000 to 5000Å; the middle etch stop layer has a thickness of from about 400 to 600Å; the

middle dielectric material layer has a thickness of from about 3000 to 5000Å; and the upper dielectric layer has a thickness of from about 400 to 600Å.

10. (original) The method of claim 1, further including the step of forming a patterned dual damascene structure within the dual damascene opening.

11. (original) The method of claim 1, wherein the opening has a width of from about 0.07 to 0.25μm.

12. (original) The method of claim 1, wherein the opening has a width of from about 0.11 to 0.20μm.

13. (original) The method of claim 1, wherein the opening has a width and a length and the width is greater than the length.

14. (original) A method of forming an aligned dual damascene opening, comprising the sequential steps of:

providing a structure having a metal structure formed thereover;

forming a layer stack over the metal structure; the layer stack comprising, in ascending order: a bottom etch stop layer; a lower dielectric material layer; a

middle etch stop layer; a middle dielectric material layer; and an upper dielectric layer;

patterning the upper dielectric layer to form a rectangular-shaped opening exposing opposing portions of the underlying middle dielectric material layer; the rectangular-shaped opening having a width and a length;

forming a patterned mask layer over the patterned upper dielectric layer, filling the opposing ends of the length of the rectangular-shaped opening and leaving exposed portions of the patterned upper dielectric layer;

patterning the middle dielectric material layer to form an opening therein using the patterned mask layer and the exposed portions of the upper dielectric layer as masks; the middle dielectric material layer opening exposing a portion of the middle etch stop layer;

removing the middle etch stop layer at its exposed portion to form a patterned middle etch stop layer having an opening exposing a portion of the lower dielectric material layer;

simultaneously patterning:

the patterned middle dielectric material layer using the patterned mask layer and the patterned upper dielectric layer as masks to form an inchoate upper trench opening; and

the lower dielectric material layer using the patterned middle etch stop layer as a mask to form an inchoate lower via opening aligned with the

inchoate upper trench opening; the inchoate lower via opening exposing a portion of the underlying bottom etch stop layer;

removing the patterned mask layer; and

removing the patterned upper dielectric material layer, the exposed portions of the patterned middle etch stop layer and the exposed portion of the bottom etch stop layer to convert:

the inchoate upper trench opening into a final upper trench opening; and

the inchoate lower via opening into a final lower via opening;

to form the aligned dual damascene opening.

15. (original) The method of claim 14, wherein the structure is a semiconductor wafer.

16. (original) The method of claim 14, wherein the structure is comprised of silicon or germanium.

17. (original) The method of claim 14, wherein the metal structure is comprised of copper, aluminum, gold, an aluminum copper alloy or an aluminum silica copper alloy; the bottom etch stop layer is comprised of a dielectric material such as SiN, SiC, SiCO, SiCN, a combination of SiC(O) and SiC(N) or BLOK; the lower dielectric

material layer is comprised of a dielectric material such as FTEOS or low-k dielectric materials; the middle etch stop layer is comprised of a dielectric material such as SiN, SiC(O), SiC(N), , a combination of SiC(O) and SiC(N) or BLOK; the middle dielectric material layer is comprised of a dielectric material such as FTEOS or low-k dielectric materials; and the upper dielectric layer is comprised of a dielectric layer such as SiN, SiC(O), SiC(N), , a combination of SiC(O) and SiC(N) or BLOK.

18. (original) The method of claim 14, wherein the metal structure is comprised of copper; the bottom etch stop layer is comprised of a combination of SiC(O) and SiC(N); the lower dielectric material layer is comprised of FTEOS or a low-k dielectric material; the middle etch stop layer is comprised of SiN; the middle dielectric material layer is comprised of FTEOS or a low-k dielectric material; and the upper dielectric layer is comprised of SiN.

19. (original) The method of claim 14, wherein the lower and middle dielectric layers are comprised of the same material.

20. (original) The method of claim 14, wherein the bottom etch stop layer, the middle etch stop layer and the upper dielectric layer are comprised of the same material.

21. (original) The method of claim 14, wherein the metal structure has a thickness of from about 1000 to 5000Å; the bottom etch stop layer has a thickness of from about 250 to 1000Å; the lower dielectric material layer has a thickness of from about 2000 to 6000Å; the middle etch stop layer has a thickness of from about 250 to 1000Å; the middle dielectric material layer has a thickness of from about 2000 to 6000Å; and the upper dielectric layer has a thickness of from about 250 to 1000Å.

22. (original) The method of claim 14, wherein the metal structure has a thickness of from about 2000 to 3000Å; the bottom etch stop layer has a thickness of from about 400 to 600Å; the lower dielectric material layer has a thickness of from about 3000 to 5000Å; the middle etch stop layer has a thickness of from about 400 to 600Å; the middle dielectric material layer has a thickness of from about 3000 to 5000Å; and the upper dielectric layer has a thickness of from about 400 to 600Å.

23. (original) The method of claim 14, further including the step of forming a patterned dual damascene structure within the dual damascene opening.

24. (original) The method of claim 14, wherein the rectangular-shaped opening has a width of from about 0.07 to 0.25μm and a length of from about 0.06 to 0.24μm.

25. (original) The method of claim 14, wherein the rectangular-shaped opening has a width of from about 0.11 to 0.20μm and a length of from about 0.10 to 0.19μm.

26. (original) A method of forming an aligned dual damascene opening, comprising the sequential steps of:

providing a structure having a metal structure formed thereover;

forming a layer stack over the metal structure; the layer stack comprising, in ascending order: a bottom etch stop layer; a lower dielectric material layer; a middle etch stop layer; a middle dielectric material layer; and an upper dielectric layer;

patterning the upper dielectric layer to form a rectangular-shaped opening exposing opposing portions of the underlying middle dielectric material layer; the rectangular-shaped opening having a width of from about 0.07 to 0.25μm and a length of from about 0.06 to 0.24μm;

forming a patterned mask layer over the patterned upper dielectric layer, filling the opposing ends of the length of the rectangular-shaped opening and leaving exposed portions of the patterned upper dielectric layer;

patterning the middle dielectric material layer to form an opening therein using the patterned mask layer and the exposed portions of the upper dielectric layer as masks; the middle dielectric material layer opening exposing a portion of the middle etch stop layer;

removing the middle etch stop layer at its exposed portion to form a patterned middle etch stop layer having an opening exposing a portion of the lower dielectric material layer;

simultaneously patterning:

the patterned middle dielectric material layer using the patterned mask layer and the patterned upper dielectric layer as masks to form an inchoate upper trench opening; and

the lower dielectric material layer using the patterned middle etch stop layer as a mask to form an inchoate lower via opening aligned with the inchoate upper trench opening; the inchoate lower via opening exposing a portion of the underlying bottom etch stop layer;

removing the patterned mask layer; and

removing the patterned upper dielectric material layer, the exposed portions of the patterned middle etch stop layer and the exposed portion of the bottom etch stop layer to convert:

the inchoate upper trench opening into a final upper trench opening; and

the inchoate lower via opening into a final lower via opening;

to form the aligned dual damascene opening.

27. (original) The method of claim 26, wherein the structure is a semiconductor wafer.

28. (original) The method of claim 26, wherein the structure is comprised of silicon or germanium.

29. (original) The method of claim 26, wherein the metal structure is comprised of copper, aluminum, gold, an aluminum copper alloy or an aluminum silica copper alloy; the bottom etch stop layer is comprised of a dielectric material such as SiN, SiC, SiCO, SiCN, a combination of SiC(O) and SiC(N) or BLOK; the lower dielectric material layer is comprised of a dielectric material such as FTEOS or low-k dielectric materials; the middle etch stop layer is comprised of a dielectric material such as SiN, SiC(O), SiC(N), , a combination of SiC(O) and SiC(N) or BLOK; the middle dielectric material layer is comprised of a dielectric material such as FTEOS or low-k dielectric materials; and the upper dielectric layer is comprised of a dielectric layer such as SiN, SiC(O), SiC(N), , a combination of SiC(O) and SiC(N) or BLOK.

30. (original) The method of claim 26, wherein the metal structure is comprised of copper; the bottom etch stop layer is comprised of a combination of SiC(O) and SiC(N); the lower dielectric material layer is comprised of FTEOS or a low-k dielectric material; the middle etch stop layer is comprised of SiN; the middle dielectric material layer is comprised of FTEOS or a low-k dielectric material; and the upper dielectric layer is comprised of SiN.

31. (original) The method of claim 26, wherein the metal structure has a thickness of from about 1000 to 5000Å; the bottom etch stop layer has a thickness of from about 260 to 1000Å; the lower dielectric material layer has a thickness of from about 2000 to 6000Å; the middle etch stop layer has a thickness of from about 250 to 1000Å; the middle dielectric material layer has a thickness of from about 2000 to 6000Å; and the upper dielectric layer has a thickness of from about 250 to 1000Å.

32. (original) The method of claim 26, wherein the metal structure has a thickness of from about 2000 to 3000Å; the bottom etch stop layer has a thickness of from about 400 to 600Å; the lower dielectric material layer has a thickness of from about 3000 to 5000Å; the middle etch stop layer has a thickness of from about 400 to 600Å; the middle dielectric material layer has a thickness of from about 3000 to 5000Å; and the upper dielectric layer has a thickness of from about 400 to 600Å.

33. (original) The method of claim 26, further including the step of forming a patterned dual damascene structure within the dual damascene opening.

34. (original) The method of claim 26, wherein the rectangular-shaped opening has a width of from about 0.11 to 0.20μm and a length of from about 0.10 to 0.19μm.